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**Preliminary version**

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**TCC807x Hardware**

**Application Note**

**for PDN Specification on Board**

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# Introduction

This document provides the DC and AC specifications of the Power Delivery Network (PDN) for the target board.

The DC PDN specification is defined by the DC resistance, which is the PDN impedance at zero frequency.

The AC PDN specification is defined by the target impedance, which is the maximum allowable PDN impedance in the specific frequency range. the PDN of the board does not affect the PDN impedance above 100 MHz so the relevant frequency range is 1–100 MHz.

Figure 1.1 shows a graph of the typical PDN specification and the board’s impedance profile.



Figure 1.1 Typical PDN Specification and Impedance Profile

# PDN Specification

## Features

Table 2.1 and Table 2.2 describe DC and AC PDN specifications of power domains in TCC8070 and TCC8071 as follows:

* VDD075D\_CORE: Internal digital core power
* VDD095D\_CPUMC\_WRAP: Power of main cluster wrapper/DSU
* VDD095D\_CPUMC\_76\_CORE0: Power of main cluster cortex-A76 core0
* VDD095D\_CPUMC\_76\_CORE1: Power of main cluster cortex-A76 core1
* VDD095D\_CPUMC\_76\_CORE2: Power of main cluster cortex-A76 core2
* VDD095D\_CPUMC\_76\_CORE3: Power of main cluster cortex-A76 core3
* VDD095D\_CPUMC\_55\_CORE0–3: Power of main cluster cortex-A55 core0–3
* VDD095D\_CPUSC\_55\_CORE0–1: Power of sub-cluster cortex-A55 core0–1
* VDD095D\_CPUSC\_WRAP: Power of sub-cluster wrapper/DSU
* VDD085D\_NPU: NPU sub-system
* VDD085D\_DDR0: Power of DDR0 controller and DDRPHY logic
* VDD085D\_DDR1: Power of DDR1 controller and DDRPHY logic
* VDD075D\_GPU: Power of graphic sub-system
* VDD075D\_DDI: Power of display sub-system
* VDD095D\_VPU: Power of video sub-system

**Note:** When designing a board, the power domains can be merged to reduce the number of voltage regulator modules (VRM) on the board. In the case of Telechips' TCC807x reference boards, some power domains are merged. The power topology of the reference boards is as follows:

|  |  |
| --- | --- |
| **Power Supply Rails** | **Power Domains of TCC807x** |
| CORE\_0P75 | * VDD075D\_CORE * VDD075D\_DDI |
| CPUMC\_0P95\_1CPU Power 1 | * VDD095D\_CPUMC\_76\_CORE0–1 |
| CPUMC\_0P95\_2CPU Power 2 | * VDD095D\_CPUMC\_76\_CORE2–3 |
| CPUMC\_0P95\_3CPU Power 3 | * VDD095D\_CPUMC\_55\_CORE0–3 |
| CPUSC\_0P95CPU Power 4 | * VDD095D\_CPUMC\_WRAP * VDD095D\_CPUSC\_55\_CORE0–1 * VDD095D\_CPUSC\_WRAP |
| NPU\_0P85NPU Power | * VDD085D\_NPU |
| IP\_0P85DDR Controller Power | * VDD085D\_DDR0–1 |
| GB\_0P75Video Power 1 | * VDD075D\_GPU |
| TC\_VB\_0P95Video Power 2 | * VDD095D\_VPU |

### TCC8070

Table 2.1 DC and AC PDN Specifications of Power Domains in TCC8070

| **Power Name of TCC8070** | **Ball Number** | **DCR [mΩ]** | | **Ztarget [mΩ]** | |
| --- | --- | --- | --- | --- | --- |
| **VRM Output to Power Ball Group of AP** | **Sense Point to Power Ball Group of AP** | **1 MHz to 20 MHz** | **20 MHz to 100 MHz** |
| VDD075D\_CORE | R17 P18 N19 T20 R21 U21 R23 R25 T26 R27 P28 AB28 N29 R29 U29 AA29 T30 Y30 AB30 W31 V32 Y32 | 5.2 | 3.8 | 14 | 66 |
| VDD095D\_CPUMC\_76\_CORE0 | AG29 AF30 AC31 AE31 AB32 AD32 AA33 AC33 Y34 AB34 AA35 Y36 W37 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE1 | AL29 AN29 AK30 AM30 AT30 AL31 AR31 AU31 AP32 AT32 AN33 AR33 AP34 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE2 | AR19 AP20 AN21 AR21 AF22 AH22 AK22 AM22 AP22 AE23 AG23 AJ23 AH24 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE3 | AM24 AT24 AL25 AN25 AR25 AT26 AR27 AT28 AR29 AU29 AV30 AW33 AV34 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_55\_CORE0–3 | AE27 AD28 AF28 AE29 AL27 AN27 AM28 AP28 | 14.7 | 5.1 | 29 | 199 |
| VDD095D\_CPUMC\_WRAP | AG25 AH26 AG27 AJ27 AH28 AJ31 | 18 | 7.2 | 35 | 187 |
| VDD095D\_CPUSC\_55\_CORE0–1 | V28 W29 V24 W25 | 31.5 | 12.6 | 58 | 210 |
| VDD095D\_CPUSC\_WRAP | N31 Y26 W27 | 83.3 | 33.3 | 88 | 220 |
| VDD085D\_NPU | AH12 AM12 AT12 AG13 AJ13 AL13 AR13 AH14 AK14 AP14 AG15 AJ15 AN15 AR15 AF16 AH16 AM16 AP16 AG17 AL17 AN17 AK18 AM18 AJ19 AL19 AK20 | 5.4 | 1 | 11 | 67 |
| VDD085D\_DDR0 | L31 M32 T32 L33 R33 U33 K34 P34 T34 W35 V36 | 39.4 | 15.7 | 52 | 128 |
| VDD085D\_DDR1 | AH32 AK32 AG33 AJ33 AF34 AH34 AE35 AG35 AD36 AF36 AE37 | 39.4 | 15.7 | 52 | 128 |
| VDD075D\_GPU | Y10 AB10 W11 AA11 AE11 V12 Y12 AD12 W13 AC13 AE13 V14 AB14 AD14 R15 U15 AA15 AC15 T16 Y16 AB16 W17 AA17 AE17 V18 Y18 AD18 AF18 W19 AC19 AE19 AB20 AD20 | 4 | 1.9 | 10 | 58 |
| VDD075D\_DDI | K18 M18 L19 K20 M20 K22 | 49.3 | 19.7 | 55 | 160 |
| VDD095D\_VPU | AM34 AL35 AN35 AU35 AM36 AT36 AR37 AU37 AP38 AT38 AN39 AR39 AM40 AP40 | 16.5 | 6.6 | 24 | 131 |

**Note 1:**

* DCR (VRM Output to Power Ball Group of AP): This is the DC resistance of the path from VRM output to power ball group of TCC8070. Refer to Figure 2.1.
* DCR (Sense Point to Power Ball Group of AP): This is the DC resistance of the path from sense point to power ball group of TCC8070. Refer to Figure 2.1.

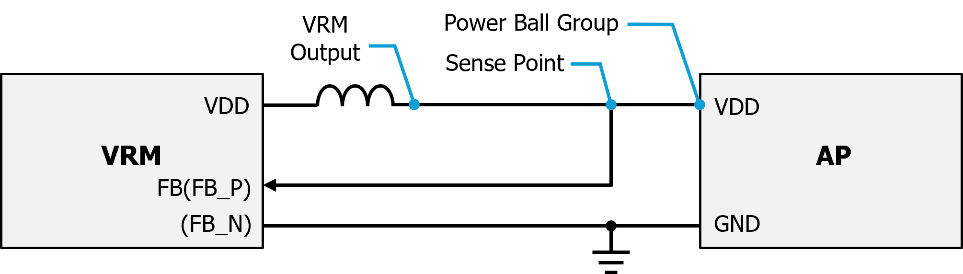


Figure 2.1 Block Diagram of Power Supply System

**Note 2:** When remote sensing is not used, DCR (VRM Output to Power Ball Group of AP) can be used for DC PDN specification.

### TCC8071

Table 2.2 DC and AC PDN Specifications of Power Domains in TCC8071

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Power Name of TCC8071** | **Ball Number** | **DCR [mΩ]** | | **Ztarget [mΩ]** | |
| **VRM Output to Power Ball Group of AP** | **Sense Point to Power Ball Group of AP** | **1 MHz to 20MHz** | **20 MHz to 100 MHz** |
| VDD075D\_CORE | R17 P18 N19 T20 R21 U21 R23 R25 T26 R27 P28 AB28 N29 R29 U29 AA29 T30 Y30 AB30 W31 V32 Y32 | 5.2 | 3.8 | 14 | 66 |
| VDD095D\_CPUMC\_76\_CORE0 | AE23 AJ23 AP20 AF22 AK22 AP22 AG23 AM22 AR19 AH22 AN21 AR21 AH24 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE1 | AL29 AN29 AK30 AM30 AT30 AL31 AR31 AU31 AP32 AT32 AN33 AR33 AP34 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE2 | AA33 AC33 AG29 AA35 AD32 W37 AB32 AE31 Y34 AB34 AF30 Y36 AC31 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_76\_CORE3 | AM24 AT24 AL25 AN25 AR25 AT26 AR27 AT28 AR29 AU29 AV30 AW33 AV34 | 16.2 | 6 | 31 | 92 |
| VDD095D\_CPUMC\_55\_CORE0–3 | AE27 AD28 AF28 AE29 AL27 AN27 AM28 AP28 | 14.7 | 5.1 | 29 | 199 |
| VDD095D\_CPUMC\_WRAP | AG25 AH26 AG27 AJ27 AH28 AJ31 | 18 | 7.2 | 35 | 187 |
| VDD095D\_CPUSC\_55\_CORE0–1 | V28 W29 V24 W25 | 31.5 | 12.6 | 58 | 210 |
| VDD095D\_CPUSC\_WRAP | Y26 W27 U27 | 83.3 | 33.3 | 88 | 220 |
| VDD085D\_NPU | AH12 AM12 AT12 AG13 AJ13 AL13 AR13 AH14 AK14 AP14 AG15 AJ15 AN15 AR15 AF16 AH16 AM16 AP16 AG17 AL17 AN17 AK18 AM18 AJ19 AL19 AK20 | 5.4 | 1 | 11 | 67 |
| VDD085D\_DDR0 | L31 M32 T32 L33 R33 U33 K34 P34 T34 W35 V36 | 39.4 | 15.7 | 52 | 128 |
| VDD085D\_DDR1 | AH32 AK32 AG33 AJ33 AF34 AH34 AE35 AG35 AD36 AF36 AE37 | 39.4 | 15.7 | 52 | 128 |
| VDD075D\_GPU | Y10 AB10 W11 AA11 AE11 V12 Y12 AD12 W13 AC13 AE13 V14 AB14 AD14 R15 U15 AA15 AC15 T16 Y16 AB16 W17 AA17 AE17 V18 Y18 AD18 AF18 W19 AC19 AE19 AB20 AD20 | 4 | 1.9 | 10 | 58 |
| VDD075D\_DDI | K18 M18 L19 K20 M20 K22 | 49.3 | 19.7 | 55 | 160 |
| VDD095D\_VPU | AM34 AL35 AN35 AU35 AM36 AT36 AR37 AU37 AP38 AT38 AN39 AR39 AM40 AP40 | 16.5 | 6.6 | 24 | 131 |

**Note 1:**

* DCR (VRM Output to Power Ball Group of AP): This is the DC resistance of the path from VRM output to power ball group of TCC8071. Refer to Figure 2.1..
* DCR (Sense Point to Power Ball Group of AP): This is the DC resistance of the path from sense point to power ball group of TCC8071. Refer to Figure 2.1..

**Note 2:** When remote sensing is not used, DCR (VRM Output to Power Ball Group of AP) can be used for DC PDN specification.

# References

1. Contact Telechips for more details: [sales@telechips.com](mailto:sales@telechips.com)
2. TCC807x Chip Specification

**Note:** Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

# Revision History

## Rev. 0.10: 2025-04-10

* Updated
* Chapter 1: Description
* Added
* Chapter 2.1: TCC8070 and TCC8071
* Changed
* Document title from “*TCC807x ~~Common~~ Hardware-Application Note for PDN Specification on Board*”

## Rev. 0.01: 2023-04-05

* Preliminary version release

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